**Tutorial 8:** WRES1201 – Computer System Architecture

1. Explain the function of the EU (execution unit) and the BIU (bus interface unit).

2. Why does pipelining improve performance?

3. What is pipeline latency?

4.

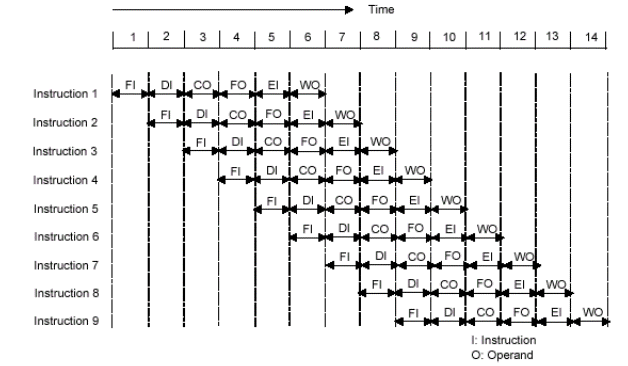


Figure 1

Consider the timing diagram of Figure 1. Assume that there is only a two stage pipeline (fetch, execute). Redraw the diagram to show how many time units are now needed for four instruction. What is *speedup* *2-stage pipeline* comparing with sequential pipelined.

5. How many time units are needed to execute 600 instructions with 6-stage pipeline. And how many time units if unpipelined. . Calculate the *speedup*.

6. Given an unpipelined processor with 10ns cycle time and pipeline latches with 0.5ns latency, what are the cycle times of pipelined versions of the processor with 2, 4, 8, and 16 stages if the datapath logic is evenly divided among the pipeline stages? Also, what is the latency of each of the pipelined versions of processor?

7. List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instruction.